ads

NOISEMAKER IC©

MANUAL

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- software notes

Ackerman Digital Systems, Inc., 110 N. York Road, Suite 208, Elmhurst, Illinois 60126 (312) 530-8992

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I. INTRODUCTION

The AY-3-8910 Programmable Sound Generator (PSG) is a large scale integrated circuit which can produce a wide variety of complex sounds under software control. After initialization of the registers in the PSG, sounds can continue to be produced while allowing the processor to do other tasks.

The AY-3-8910 has three 12 bit tone generators: one 4 bit amplitude control for each of the three tone sources, one 5 bit noise generator, and one 16 bit envelope generator. As an added feature, the AY-3-8910 has two 8 bit Input/Output (I/O) ports which are brought out for user applications.

The techniques described in this manual will produce a wide variety of results. However, since the range of sounds to be synthesized are so vast, this manual should only be viewed as an introduction to the capabilities of the ADS Noisemaker][.

II. BOARD CONSTRUCTION

1. Examine the ADS Noisemaker][for shorts. If an ohmmeter is available, measure between address lines, data lines, and the +5 volt and ground lines for shorts.

2. Noting the orientation against the silk screen, install and solder the I/C sockets.

3. Carefully observing the polarized capacitors orientation against the silk screen, install and solder the capacitors.

4. Install and solder the resistors and Molex speaker connector.

5. Inspect the board for any possible solder bridges or cold solder joints.

6. Apply power to the board and verify that between 4.8 and 5.2 volts are available to the board (Capacitor C7.)

7. Remove power and install the I/C's. (Do not bend any pins and/or reverse the I/C's in their sockets.)

8. Set volume (R1) midway.

9. Connect the Apple II speaker to the Molex connector.

10. Install the board and verify that your computer and other I/O ports function normally.

III. USING THE ADS NOISEMAKER][

The AY-3-8910 PSG is programmed through two I/O addresses. Before one of the sixteen internal registers can be read from or written to, it must first be selected by writing a number (0-15) into the PSG Address Register. (Diagram 1, Page 2.) The selected Data Register can then be read from or written to until another PSG Data Register is selected. (See e.g. 1, Page 2.)

e.g. 1

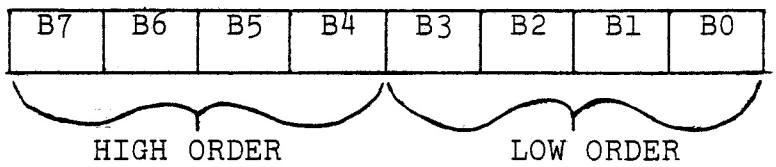
The PSG Address Register and Data Register are located in Slot #0 at CØ8Ø and CØ81 respectively. The PSG Address and Data Registers located in Slot #1 are at CØ9Ø and CØ91 respectively.

Below are the general equations which define the locations of the Address Register and its corresponding Data Register.

Equation 1 Address Register $C0\emptyset\emptyset_{16}$ + (Slot # * 16)

Equation 2 Data Register $C0\emptyset\emptyset_{16}$ + (Slot # * 16) + 1

Diagram 1 - Address Register (Pointer Register)



To produce a tone, you must:

1. Select the Enables Register (R7) (See Fig. 1, Page 8)
2. Load R7 with hex FE (Tone-Out Channel A)
3. Select the Channel A Amplitude Register (R8)
4. Load R8 with hex ØF (Maximum Output)
5. Select the Channel A Fine Tune Register (R0) (Fig. 1, Page 8)
6. Load R0 with hex 8Ø (Audible Tone)

The four Low Order address bits (B3-B0) select one of 16 Data Registers (R0-R15.) The four High Order address bits (B7-B4) are not used. In the B7-B4 locations, the Address Register will only recognize 0000.

Below is a sample program which generates a simple tone on one of the three channels in the PSG. This program is written at starting address Ø3ØØ and access slot #1 in your Apple II.

	FOR USE WITH 8T28 BUFFERS			FOR USE WITH 8T26 BUFFERS		
3ØØ	A9 Ø7	LDA #$Ø7	-Select Enable Reg.	A9 F8	LDA #$F8	
3Ø2	8D 9Ø CØ	STA $C090	R7 and Load With	8D 9Ø CØ	STA $CØ9Ø	
3Ø5	A9 FE	LDA #$FE	FE (Enable Tone	A9 Ø1	LDA #$Ø1	
3Ø7	8D 91 CØ	STA $CØ91	Channel A)	8D 91 CØ	STA $CØ91	
3ØA	A9 Ø8	LDA #$Ø8	-Select Channel A	A9 F7	LDA #$F7	
3ØC	8D 9Ø CØ	STA $CØ9Ø	Amplitude Reg. R8	8D 9Ø CØ	STA $CØ9Ø	
3ØF	A9 ØF	LDA #$ØF	and Load With ØF	A9 FØ	LDA #$FØ	
311	8D 91 CØ	STA #CØ91	(Max. Amplitude)	8D 91 CØ	STA $CØ91	
314	A9 ØØ SWEEP	LDA #$ØØ	-Select Fine Tune	A9 FF SWEEP	LDA #$FF	
316	8D 9Ø CØ	STA $CØ9Ø	Reg. R0 and Load	8D 9Ø CØ	STA $CØ9Ø	
319	A9 8Ø	LDA #$8Ø	With 8Ø (Audible	A9 8Ø	LDA #$8Ø	
31B	8D 91 CØ	STA $CØ91	Frequency)	8D 91 CØ	STA $CØ91	
31E	4C 1E Ø3	JMP $Ø31E	-Infinite Loop	4C 1E Ø3	JMP $Ø31E	

The sample program on page 2 may be modified slightly to produce a more complex sound. To modify, start at address Ø319 and add the following changes:

```
Ø319  E8       DELAY  INX          -Wait Approx. 1 ms.   E8     DELAY  INX
Ø31A  DØ FD           BNE DELAY                          DØ FD         BNE DELAY
Ø31C  CE 91 CØ        DEC $CØ91    -Decrement Value      EE 91 CØ      INC $CØ91
Ø31F  DØ F8           BNE DELAY     in Channel A Tone    DØ F8         BNE DELAY
Ø321  A9 Ø8           LDA #$Ø8     -Select Amplitude     A9 F7         LDA #$F7
Ø323  8D 9Ø CØ        STA $CØ9Ø     Register R8          8D 9Ø CØ      STA $CØ9Ø
Ø326  CE 91 CØ        DEC $CØ91    -Decrement Amplitude  EE 91 CØ      INC $CØ91
Ø329  DØ E9           BNE SWEEP     by 1 Bit             DØ E9         BNE SWEEP
Ø32B  4C ØA Ø3        JMP $Ø3ØA    -Jump and Do Again    4C ØA Ø3      JMP $Ø3ØA
```

To utilize the noise generator, simply modify the entire program by placing F6 at address Ø3Ø6 if using the 8T28 Buffer or Ø9 at Ø3Ø6 if using the 8T26 Buffer.

When producing software for the PSG on the ADS Noisemaker][, it is often necessary to read data from the Data Register array. Reading can be done in a similar manner to writing to the Data Register array, but efforts must be taken in software to mask off any "not used" bits in a Data Register (R0-R15, Fig. 1, Page 8) because General Instruments dosn't guarantee "not used" bits to be "0" or "1". The Address Register in the PSG looks like a write only register to the CPU, therefore, it is impossible to read data from the Address Register.

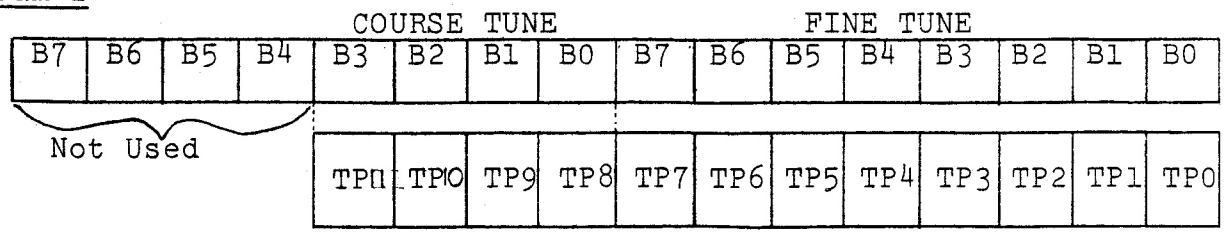
Keeping these guidelines in mind along with the equations in the next section will help you produce an almost limitless variety of sounds all under software control.

IV. ARCHITECTURE AND EQUATIONS GOVERNING THE PSG

(a) TONE GENERATOR CONTROL

The frequency of each square wave generated by the three tone generators (Channels A, B and C) is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 12 bit tone period value. Each 12 bit value is obtained in the PSG by combining the contents of the relative Course and Fine Tune Register (Defined in Diagram 3) and illustrated in Fig. 1, Page 8 and Diagram 2 below.

Diagram 2



12 Bit Tone Period (TP) to Tone Generator

Diagram 3

CHANNEL	COARSE TUNE RREGISTER	FINE TUNE REGISTER
A	R1	R0
B	R3	R2
C	R5	R4

The equations listed below define tone frequency.

Tone Frequency $f_t = f_{clock} / (16 * TP10)$ where f_{clock} = frequency of clock (Note Schematic on Page 9)

Eq. 3 $TP_{10} = 256\ CT_{10} + FT_{10}$ (Decimal equivalent of Tone Period)

CT_{10} defines the decimal equivalent of Coarse Tune Reg.

FT_{10} defines the decimal equivalent of Fine Tune Reg.

(b) **NOISE GENERATOR CONTROL** (Register R6)

The frequency of the noise source is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 5 bit noise period value. This 5 bit value consists of the lower 5 bits (B4-B0) of Register R6. (Illustrated in Diagram 4 below.)

Diagram 4

Register R6

B7	B6	B5	B4	B3	B2	B1	B0
NOT USED			5 Bit Noise Period (NP)				

Note: The 5 bit value in R6 is a period value. Therefore, the higher the value in the register, the lower the resultant noise frequency.

Eq. 4 Noise Frequency $F_n = f_{clock} / (16NP_{10})$

NP defines decimal equivalent of the Noise Period Register.

(c) **ENABLE CONTROL** (Register R7)

This is a multi-function register which controls the three noise/tone mixers and two general purpose I/O ports.

The mixers as noted above combine the noise and tone frequencies for each of the three channels. The determination of combining neither, either, or both noise and tone frequencies on each channel is made by the state of bits B5-B0 of R7. (See Diagram 5 below.)

Diagram 5

Register R7

B7	B6	B5	B4	B3	B2	B1	B0
$\overline{\text{Input Enable}}$		$\overline{\text{Noise Enable}}$			$\overline{\text{Tone Enable}}$		
B	A	C	B	A	C	B	A

Note: These Registers are Negative True

The direction (In or Out) of the two general purpose I/O ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7.

A logic level of "0" entered in the Noise and/or Tone Enable Register will activate the noise and/or tone for that channel. A logic level of "1" entered in the Noise and/or Tone Enable Register will deactivate that noise and/or tone.

A logic level of "0" written into the I/O Enable Register will place that/those ports into the input mode. A logic level of "1" written into the Input Enable Register will place that/those ports into the output mode.

Note that the disabling noise and tone does not turn off a channel. A high frequency envelope would be heard as a tone or a series of clicks. Turning a channel off can only be accomplished by writing zeroes into the Amplitude Control Registers described next.

(d) **AMPLITUDE CONTROL**

The amplitudes of the signals generated by each of the three D/A converters (one for each channel) is determined by the contents of the lower 5 bits (B4-B0) of Registers R8, R9 and R10. (See Fig. 1, Page 8.)

M-0 Amplitude is fixed at one of 16 levels as determined by L3, L2, L1 and L0

M-1 Amplitude is variable at 16 levels as determined by the output of the generator. (Note Fig. 3, Page 8.)

(e) **ENVELOPE PERIOD CONTROL**

To accomplish the generation of fairly complex envelope patterns, two independent methods of control are provided in the PSG. First, it is possible to vary the frequency of the envelope using Registers R11 and R12 and second, the relative shape and cycle pattern of the envelope can be varied using Register R13. The following paragraphs first describe the envelope period control and then the envelope shape/cycle control.

The frequency of the envelope is obtained in the PSG by first counting down the input clock by 256, then by further counting down the result by the programmed 16 bit envelope period value. This 16 bit value is obtained in the PSG by combining the contents of the Envelope Coarse and Fine Tune Registers. (See Diagram 6 below.)

Diagram 6

R12 - COARSE TUNE REGISTER							R11 - FINE TUNE REGISTER								
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0

EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP 9	EP 8	EP 7	EP 6	EP 5	EP 4	EP 3	EP 2	EP 1	EP 0

16 Bit Envelope Period (EP)

Note that the 16 bit value programmed in the combined Coarse and Fine Tune Registers is a period value; therefore, the higher the value in the register, the lower the resultant envelope frequency.

Eq. 5 Envelope Frequency $F_e = f_{clock} / 256\ EP_{10}$

$EP_{10} = 256\ CT_{10} + FT_{10}$ (Decimal Equivalent of Envelope Period)

CT_{10} defines the decimal equivalent of the Coarse Tune Register

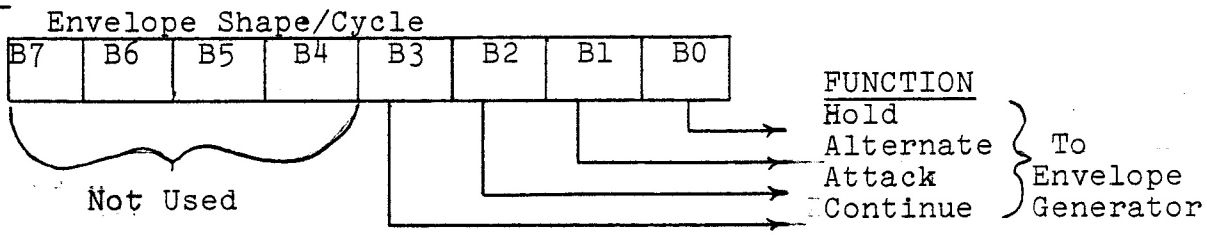
FT_{10} defines the decimal equivalent of the Fine Tune Register

(f) ENVELOPE SHAPE/CYCLE CONTROL

The envelope generator further counts down the envelope frequency by 16, producing a 16 state per cycle envelope pattern as defined by its 4 bit counter output, E3, E2, E1, and E0. The particular shape and cycle pattern of any desired envelope is determined by controlling the count pattern (count up/count down) of the 4 bit counter and by defining a single-cycle or repeat-cycle pattern.

This Envelope Shape/Cycle Control is contained in the lower 4 bits (B3-B0) of Register 13. Each of these 4 bits controls a function in the envelope generator. (See Diagram 7 below.)

Diagram 7



ENVELOPE SHAPE/CYCLE DEFINITIONS

HOLD When Logic "1", limits the envelope to one cycle, holding the last count of the envelope counter (E3-E0=0000 or 1111) depending on whether the envelope counter was in a count down or count up mode.

ALTERNATE When Logic "1", the envelope counter reverses count direction (up-down) after each cycle.

ATTACK When Logic "1", the envelope counter will count up (attack) from E3, E2, E1, E0 = 0000 to E3, E2, E1, E0 = 1111; when Logic "0", the envelope counter will count down (decay) from E3, E2, E1, E0 = 1111 to E3, E2, E1, E0 = 0000.

CONTINUE When set to Logic "1", the cycle pattern will be as defined by the hold bit. When set to Logic "0", the envelope generator will reset to 0000 after one cycle and hold at that count.

Figure 2 on page 8 gives a graphic representation of the possible envelope shapes.

Note: When both the hold bit and the alternate bit are "1's", the envelope is reset to its initial count before holding.

(g) I/O PORTS

Registers R14 and R15 function as intermediate data storage registers between the PSG/CPU data bus (D0-D7) and the two I/O ports. (IOA7-IOA0 and IOB7-IOB0) Both ports are made available to the user via a 16 pin dip connector. (Note Schematic on page 9.) Using the I/O Register for data transfer will have no effect on sound generation.

To output data from the CPU bus to a peripheral deveice connected to I/O Port A requires the following steps:

1. Latch Address R7 (Select Enable Register)
2. Write Data to PSG (Setting B6 of R7 to "1")
3. Latch Address R14 (Select IOA Register)
4. Write Data to PSG (Data to be Output on I/O Port A)

To input data from I/O Port A to the CPU bus requires the following steps:

1. Latch Address R7 (Select Enable Register)
2. Write Data to PSG (Setting B6 of R7 to "0")
3. Latch Address R15 (Select IOA Register)
4. Read Data From PSG (Data From I/O Port A)

When left in the output mode, data will remain on the I/O port(s) until changed by loading different data or by resetting the PSG.

When left in the input mode, the contents of Register R14 and R15 will follow the signals applied to the I/O ports; however, transfer of this data to the CPU requires a "Read" operation.

(h) D/A CONVERTER OPERATION

Since we are trying to produce sounds for the non-linear amplitude detection mechanism of the human ear, the D/A conversion is preformed in logarithmic steps with a normalized voltage range from 0 to 1 volt. The specific amplitude control of each of the three D/A converters is accomplished by the three sets of 4 bit outputs of the amplitude control block. The mixer outputs provide the base signal frequency. (Noise and Tone)

FIGURES 1-4

REG. \ BIT	B7	B6	B5	B4	B3	B2	B1	B0
R0 Channel	8 Bit Fine Tune A							
R1 A Tone					4 Bit Coarse			
R2 Channel	8 Bit Fine Tune B							
R3 B Tone					4 Bit Coarse			
R4 Channel	8 Bit Fine Tune C							
R5 C Tone					4 Bit Coarse			
R6 Noise Per.				5 Bit Period				
R7 Enable	IN/OUT		Noise			Tone		
	IOB	IOA	C	B	A	C	B	A
R8 Amplitude A				M	L3	L2	L1	L0
R9 Amplitude B				M	L3	L2	L1	L0
R10 Amplitude C				M	L3	L2	L1	L0
R11 Envelope	8 Bit Fine Tune							
R12 Period	8 Bit Coarse Tune							
R13 Envl Shape					CONT	ATT	ALT	HOLD
R14 I/O Port A	8 Bit Parallel I/O Port							
R15 I/O Port B	8 Bit Parallel I/O Port							

Fig. 1 PSG Data Register Array

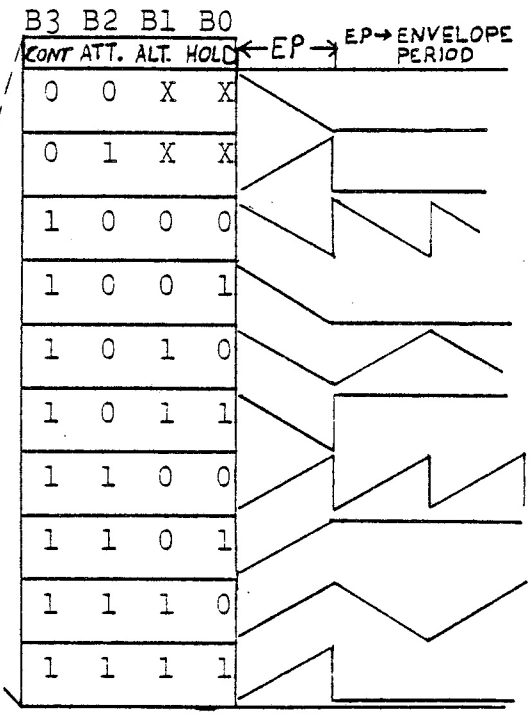


Fig. 2 Envelope Shape

Graphic representation of the decimal values of the amplitude control output.

EP= Envelope Period

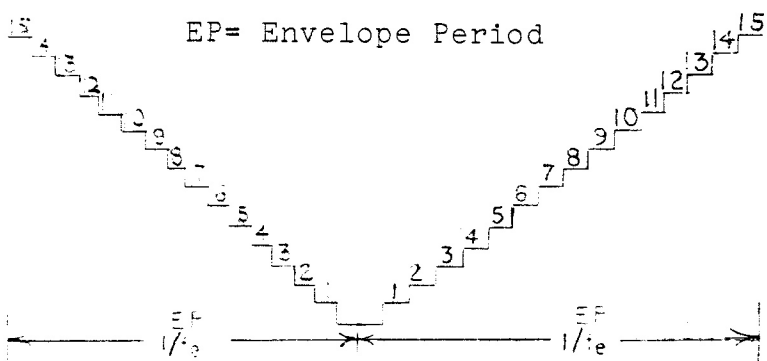


Fig. 3 Variable Amplitude Control (M=1)

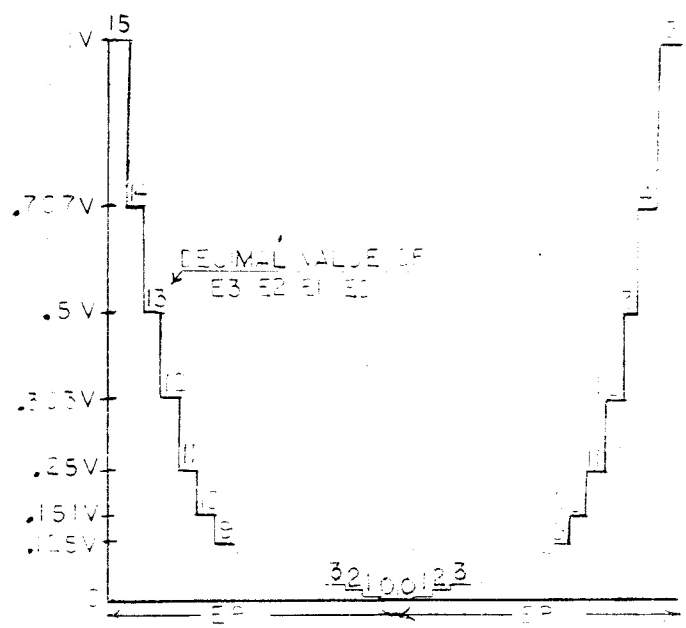
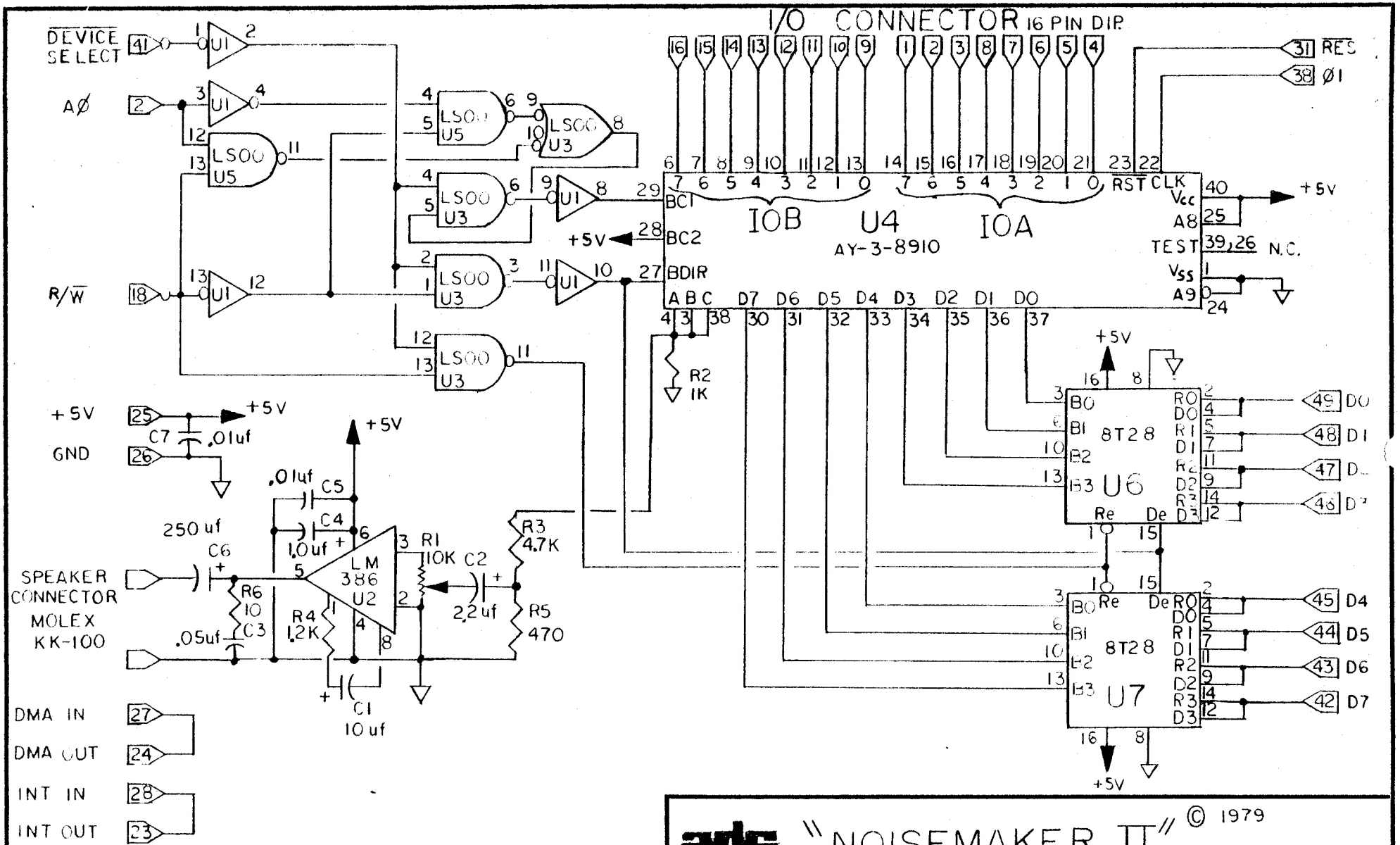


Fig. 4 D/A Converter Output



UNUSED GATES

U1 - 74LS04 PINS 5 & 6

U5 - 74LSOO PINS 1,2,3, 10, 9, 8

ads "NOISEMAKER II" © 1979

SCALE: NONE	APPROVED BY: Steven J. Ackerman	DRAWN BY D.S.
DATE: 12-10-79		REVISED 4-14-80

ALL RESISTORS 1/4 W.
ALL CAPACITORS 25 V.

PSG ADDRESS = DEVICE SELECT • A0 • R/W

PSG DATA = DEVICE SELECT • A0 • (R/W + R/W)

DRAWING NUMBER NM2 - 1

VI.

APPENDIX I

SAMPLE SOUND EFFECTS

A few of the more commonly used sounds are listed below. The first chart shows how to produce a European siren effect requiring only the use of the tone generator. A second chart describes an effect requiring only the noise and envelope generator producing a gun shot. A laser sound or a whistling bomb sound can be generated by having the processor sweep a tone channel from a starting tone to an ending tone at a defined rate. These two sounds are described in chart 3 and chart 4 respectivly. To further enhance chart 4 follow it with chart 2 after the processor has completed the tone sweep.

STEP	DATA REGISTER #	LOAD WITH HEX VALUE	EXPLANATION
1	R0	9Ø	-Set channel A tone period to 2.26ms (442 hz)
2	R1	ØØ	
3	R7	3E	-Enable tone channel A only
4	R10	ØF	-Set maximum amplitude on channel A
	Have processor wait approximatly 350 ms before continuing		
5	R0	55	-Set channel A tone period to 5.3 ms
6	R1	Ø1	

CHART 1 EUROPEAN SIREN

1	R6	ØF	-Set noise period to mid value
2	R7	Ø7	-Enable all noise generators
3	R8	1Ø	-Select amplitude under the control
4	R9	1Ø	of the envelope generator
5	R10	1Ø	
6	R12	Ø8	-Set envelope period to .524 sec.
7	R13	ØØ	-Select envelope shape for one cycle only

CHART 2 GUN SHOT

1	R7	3E	-Enable tone channel A only
2	R10	ØF	-Select maximum amplitude an channel A
3	R0 (start)	1B	-Sweep effect for channel A tone period
4	R0 (end)	38	via processor loop with approx. 5 ms. wait time between each step from 1B to 38.
5	R10	ØØ	-Turn off channel A to end sound effect.

CHART 3 LASER SOUND EFFECT

1	R7	3E	-Enable tone channel A only
2	R10	ØF	-Select maximum amplitude on channel A
3	R0 (start)	1B	-Sweep effect for channel A tone period via
4	R0 (end)	6D	a processor loop with approx. 35ms. per step

CHART 4 WHISTLING BOMB

PARTS LIST

	PART	DESCRIPTION	QUANTITY	DESIGNATION
	74LS04	Hex Inverter TTL	1	U1
	LM386N	Audio Amplifier	1	U2
	74LS00	Quad Nand Gate	2	U3 & U5
	AY-3-8910	GI Sound Generator	1	U4
*	8T28	Bi-directional Data XCVR	2	U6 & U7
***	10uf 25v	Electrolytic Cap	1	C1
***	2uf 25v	A.C. Coupling Cap	1	C2
	.05uf 25v	Low Pass Filter	1	C3
***	1uf 25v	Decoupling Cap	1	C4
	.01uf 25v	Decoupling Cap	2	C5 & C7
***	250uf 25v	A.C. Coupling Cap	1	C6
**	10K ohm	P.C. Mount Linear Pot	1	R1
	1K ohm	Current Divider	1	R2
	4.7K ohm	Voltage Divider	1	R3
	1.2K ohm	Resistor	1	R4
	470 ohm	Voltage Divider	1	R5
	10 ohm	Resistor	1	R6
	IC Socket	14 Pin Solder Tail	3	
	IC Socket	16 Pin Solder Tail	3	
	IC Socket	40 Pin Solder Tail	1	
	KK-100	Molex Connector (2 pins)	1	

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* 8T26's may be substituted for the 8T28's with inverting software.
** All resistors are 1/4 watt unless otherwise specified.
*** These capacitors may be polarized electrolytics. tollerance +80-20%